REMARKS

Claims 1-10, 12-19, 21 and 22 are pending. By this Amendment Submission, claims 1 and 12 are amended. No new matter is added by any of these amendments.

Reconsideration based on the following remarks is respectfully requested.

I. Amendment Entry with Request for Continued Examination

Entry of this amendment is proper under 37 CFR §1.114 because this Submission is filed in conjunction with a Request for Continued Examination.

II. Claims 1-10, 12-19, 21 and 22 Define Patentable Subject Matter

The Final Office Action rejects claims 1, 6-8, 10, 12, 14-17, 19, 21 and 22 under 35 U.S.C. §102(b) over U.S. Patent 5,767,009 to Yoshida *et al.* (hereinafter "Yoshida"). This rejection is respectfully traversed.

Yoshida does not teach or suggest a method of manufacture of a semiconductor device, including providing an adhesive between a surface of a semiconductor chip having a plurality of electrodes on which the electrodes are provided and a surface of a substrate having a plurality of leads and an undivided film on which the leads and the undivided film are formed, positioning at least one of the plurality of electrodes to be opposed to at least one of the plurality of leads such that the undivided film is opposed to the semiconductor chip, and applying pressure in a direction such as to make a gap between the semiconductor chip and the substrate narrower such that the adhesive extends to be disposed on the whole of the undivided film, wherein the undivided film is formed with a lower adhesion to the adhesive than a base material of the substrate, and the undivided film is broader than each of the leads at their portions opposed to the electrodes, and the undivided film is formed to be electrically isolated from both the electrodes and the leads, a region on which the adhesive is disposed includes a first region with low adhesion to the adhesive and a second region with high

adhesion to the adhesive, an area of the first region ≧ an area of the second region, as recited in claim 1.

Yoshida also does not teach or suggest a semiconductor device including a semiconductor chip having a plurality of electrodes, a substrate on which is formed a plurality of leads and an undivided film, the undivided film opposed to the semiconductor chip and electrically isolated from both the electrodes and the leads, and an adhesive provided between a surface of the semiconductor chip on which the electrodes are formed and a surface of the substrate on which the leads and the undivided film are formed to adhere the semiconductor chip and the substrate, the adhesive disposed on the whole of the undivided film, wherein at least one of the plurality of electrodes and at least one of the plurality of leads are electrically connected, and wherein the undivided film is formed with a lower adhesion to the adhesive than a base material of the substrate, and the undivided film is broader than each of the leads at their portions opposed to the electrodes, wherein a region on which the adhesive is disposed includes a first region with low adhesion to the adhesive and a second region with high adhesion to the adhesive, an area of the first region ≧ an area of the second region, as recited in claim 12.

Yoshida teaches an insulation film 16 with an electro-conductive layer 18 (assumed to correspond to the claimed "undivided film") between first and second chips 1 and 5. Yoshida further teaches that extrusions 17 are formed on the film 16, and that insulation resins 20, 22 are pressed between the film 16 and the chips 5 and 1, respectively (col. 6, lines 25-57 and Figs. 5-7 of Yoshida). There is no teaching or suggestion that the film 18 is formed to be electrically isolated from both the electrodes and the leads.

Accordingly, independent claims 1 and 12, and all claims dependint therefrom are patentably distinct from Yoshida. Withdrawl of the rejection under 35 U.S.C. §102 is respectfully requested.

The Final Office Action further rejects claims 2 and 13 under 35 U.S.C. §103(a) over Yoshida in view of Japanese Patent Application 07-169795 to Oda (hereinafter "Oda"), and claims 3-5, 9 and 18 under 35 U.S.C. §103(a) over Yoshida in view of U.S. Patent 6,548,890 to Tada *et al.* (hereinafter "Tada"). These rejections are respectfully traversed.

Oda does not compensate for the deficiencies of Yoshida outlined above for claims 1 and 12. Nor does Oda teach, disclose or suggest the additional features recited in claims 2 and 13. Instead, Oda discloses a lead-on-chip package. In particular, Oda teaches an anisotropic conductive film 108 having conductive particles 109 (Abstract of Oda).

Tada also does not compensate for the deficiencies of Yoshida outlined above for claims 1 and 12. Nor does Tada teach, disclose or suggest the additional features recited in claims 3-5, 9 and 18. Instead, Tada discloses a lead frame processing method. In particular, Tada teaches plating gold over inner leads 3 in step S151, and removing the gold plating elsewhere in step S152 (col. 15, lines 32-49 and Fig. 2 of Tada).

For at least these reasons, Applicant respectfully asserts that the independent claims are now patentable over the applied reference. The dependent claims are likewise patentable over the applied references for at least the reasons discussed as well as for the additional features they recite. Consequently, all the claims are in condition for allowance. Thus, Applicant respectfully requests that the rejections under 35 U.S.C. §§102 and 103 be withdrawn.

III. Conclusion

In view of the foregoing amendments and remarks, Applicant respectfully submits that this application is in condition for allowance. Favorable consideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further is desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,

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